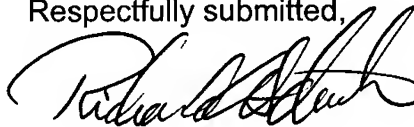


**REMARKS**

This application is a divisional application based on U.S. Application Serial No. 09/416,998 filed October 13, 1999. Claims 1-18 were elected in the parent application in response to a restriction requirement, and were allowed on November 5, 2001. Accordingly, claims 1-18 are hereby cancelled from the present application. Claims 19-40 are now pending in this application. Attached hereto is a marked-up version of the changes to be made to the application, entitled "**Version With Markings To Show Changes Made**".

Applicants also enclose herewith a check in the amount of \$776.00 to cover the filing fee for this application. The Commissioner is hereby authorized to charge any deficiency or overpayment in connection with this application to Deposit Account No. 19-1345.

Respectfully submitted,



Richard A. Schuth, Reg. No. 47,929  
SENNIGER, POWERS, LEAVITT & ROEDEL  
One Metropolitan Square, 16th Floor  
St. Louis, Missouri 63102  
(314) 231-5400

RAS/msc

\*Attachment/Enclosure

Express Mail Label No. EL 937977085 US

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE TITLE:**

The title has been amended to the following:

**THERMAL[LY] ANNEALING[ED,] PROCESS FOR PRODUCING LOW  
DEFECT DENSITY SINGLE CRYSTAL SILICON**

**IN THE SPECIFICATION:**

The paragraph beginning at line 3, page 1 has been amended to the following:

**CROSS-REFERENCE TO RELATED APPLICATION**

This **patent** application claims priority from U.S. **P[p]rovisional Patent**  
**A[a]pplication Serial No. 60/104,304, filed on October 14, 1998 and U.S. Serial No.**  
**09/416,998, filed on October 13, 1999.**

**IN THE CLAIMS:**

Claims 1-18 have been canceled.

**IN THE ABSTRACT:**

The Abstract text beginning at line 1, page 66 has been amended as follows:

A **thermal annealing process for producing a low defect density** single  
crystal silicon wafer[ **having a central axis, a front side and a back side which are  
generally perpendicular to the central axis, a central plane between the front and  
back sides, a circumferential edge, and a radius extending from the central axis  
to the circumferential edge. [The wafer comprises first and second axially  
symmetric regions].** The **process includes thermally annealing a wafer having a**  
first axially symmetric region **which** extends radially inwardly from the circumferential

edge, contains silicon self-interstitials as the predominant intrinsic point defect, and is substantially free of agglomerated interstitial defects[. **The], a second axially symmetric region which has vacancies as the predominant intrinsic point defect[, **comprises a surface]. The wafer is subjected to a thermal anneal at a temperature in excess of about 10000°C in an atmosphere of hydrogen, argon or a mixture thereof to dissolve[** layer extending from the front side toward the central plane and a bulk layer extending from the surface layer to the central plane, wherein the number density of] agglomerated vacancy defects present in the **second axially symmetric region within a layer extending from the front side toward the central plane**[ surface layer is less than the concentration in the bulk layer].**